AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method for forming a recognition mark on a substrate for a bare chip carrier of a KGD, said substrate having a front surface and a back surface ~~wherein wiring patterns are formed on a surface of one side of an insulating substrate~~, comprising the steps of:

forming wiring patterns on the front surface;

forming a conductive pattern as a recognition mark on the front surface ~~one surface where said wiring patterns are formed~~; and

forming a through hole from ~~a~~ the back surface ~~where said wiring pattern is not formed~~ toward said conductive pattern.

2. (Currently Amended) A method for forming a recognition mark on a substrate for a bare chip carrier of a KGD as claimed in claim 1, wherein said substrate is formed with a bump ~~to be connected to said KGD on the surface where said wiring pattern is not formed~~ on the back surface.

3. (Currently Amended) A method for forming a recognition mark on a substrate for a bare chip carrier of a KGD as claimed in claim 1, wherein said conductive pattern has a particular shape as said recognition mark.

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4. (Currently Amended) A method for forming a recognition mark on a substrate for a bare chip carrier of a KGD as claimed in claim 1, wherein a shape of said through hole defines said recognition mark.

5. (Currently Amended) A method for forming a recognition mark on a substrate for a bare chip carrier of a KGD as claimed in claim 4, wherein said through hole is filled with a plating material until the end of said plating lies in flush with said surface where said wiring pattern is not formed.

6. (Currently Amended) A method for forming a recognition mark on a substrate for a bare carrier of a KGD, ~~wherein wiring patterns are formed on both surfaces of an insulating substrate~~ said substrate having a front surface and a back surface, comprising the steps of:

forming wiring patterns on the front surface and the back surface;

forming a conductive pattern as a recognition mark on the front surface ~~where said wiring patterns are formed~~; and

forming a through hole from ~~a~~ the back surface~~, where said KGD is not mounted and said wiring pattern is formed,~~ toward said conductive pattern.

7. (Currently Amended) A method for forming a recognition mark on a substrate for a bare carrier of a KGD, said substrate having a plurality of layers and said plurality of layers including a back surface ~~wherein wiring patterns are formed on a plurality of layers of an insulating substrate~~, comprising the steps of:

forming wiring patterns on one or more of the layers;

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forming a conductive pattern as a recognition mark on any layer where said wiring patterns are formed; and

forming a through hole from the back surface ~~a surface of the substrate where said KGD is to be mounted~~ toward said conductive pattern;

wherein forming the conductive pattern is performed at the same time as forming the wiring patterns.

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